Part #29

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Green et al.

Serial No.: 09/172,553

Filed: October 14, 1998

For: HIGH SURFACE AREA CAPACITORS AND INTERMEDIATE STORAGE POLY STRUCTURES FORMED DURING FABRICATION THEREOF (Amended)

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APPEAL BRIEF

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Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Attn: Board of Patent Appeals and Interferences

Sir:

This Appeal Brief is being submitted in TRIPLICATE pursuant to 37 C.F.R. § 1.192(a) in the format required by 37 C.F.R. § 1.192(c) and with the fee required by 37 C.F.R. § 1.17(c).

(1) REAL PARTY IN INTEREST

U.S. Serial No. 09/172,553, the application at issue in the above-referenced appeal, has been assigned to Micron Technology, Inc. ("Assignee"). The assignment has been recorded with the United States Patent & Trademark Office ("Office") at Reel No. 8915, Frame No. 0414. Accordingly, Micron Technology, Inc. is the real party in interest in the above-referenced appeal.

(2) RELATED APPEALS AND INTERFERENCES

Neither Appellant nor the undersigned attorney is currently aware of any appeals or interference proceedings that would affect or be affected by the Board's decision in the above-referenced appeal.

(3) STATUS OF CLAIMS

Claims 31-35 and 37-45 are currently pending and under consideration in the above-referenced application.

Claims 1-30 and 36 have been canceled without prejudice or disclaimer.

No claims have been allowed.

The rejections of claims 31-35 and 37-45 are being appealed.

(4) STATUS OF AMENDMENTS

The above-referenced application was filed on October 14, 1998, with nineteen (19) claims, which included claims 16-34. Claims 1-15 were canceled by way of a Preliminary Amendment that was filed concurrently with the above-referenced application.

A first Office Action on the merits was mailed on June 30, 2000. Each of claims 16-34 was rejected in the first Office Action.

An Amendment that was responsive to the first Office Action was mailed on September 28, 2000, and granted a filing date of October 4, 2000. In addition to presenting several amendments to the specification and claims, as well as an explanation as to the patentability of the claims, new claims 35-41 were added.

The Office replied with a Restriction Requirement, dated December 29, 2000.

In a Response to the Restriction Requirement, which was mailed on January 9, 2001, and received a filing date of January 16, 2001, an election was made to prosecute claims 31-41, nonelected claims 16-30 were canceled without prejudice or disclaimer, and new claims 42-45 were added.

A Final Office Action was mailed on April 6, 2001. Each of claims 31-45 was rejected in the Final Office Action.

An Amendment Under 37 C.F.R. § 1.116 was filed on May 29, 2001. In addition to proposing several claim amendments, it was proposed that claim 36 be canceled without prejudice or disclaimer.

In an Advisory Action dated June 7, 2001, the Office declined to enter the amendments presented in the Amendment Under 37 C.F.R. § 1.116.

Accordingly, a Request for Continued Examination was filed on June 15, 2001.

The Office mailed a third Office Action on the merits on July 17, 2001. Each of the claims that remained pending, which, at this point, included claims 31-35 and 37-45, was again rejected.

An Amendment responsive to the third Office Action was filed on October 16, 2001.

On January 3, 2002, the Office mailed a fourth, nonfinal Office Action, as the rejections that were presented in the preceding Office Action had been overcome.

An Amendment in response to the fourth Office Action was sent on April 1, 2002, and received a filing date of April 12, 2002.

Another Final Office Action followed on June 25, 2002, in which the rejections of the previous, fourth Office Action were maintained.

On August 26, 2002, a second Amendment Under 37 C.F.R. § 1.116 was filed.

As indicated in an Advisory Action that was mailed on September 23, 2002, the Office refused to enter the amendments that were presented in the second Amendment Under 37 C.F.R. § 1.116.

Accordingly, on September 30, 2002, a second Request for Continued Examination was filed.

The Office mailed a sixth Office Action on October 22, 2002. The grounds for rejecting claims 31-35 and 37-45 were again changed.

Another Amendment was mailed on January 21, 2003, in response to the sixth Office Action, and received a filing date of January 27, 2003. That Amendment included explanations as to why each of the claims, as revised, was allowable over the art of record. No further amendments to the claims have been presented in the above-referenced application.

Thereafter, the Office replied with yet another Final Office Action, which was dated April 1, 2003.

Another Amendment Under 37 C.F.R. § 1.116, in which an amendment to the title was presented, was mailed on June 2, 2003, and received a filing date of June 5, 2003. The explanations as to why claims 31-35 and 37-45 are allowable were reiterated and enhanced in that Amendment.

In an Advisory Action dated June 26, 2003, the Office indicated that the amendment to the title would be entered upon the filing of a Notice of Appeal in the above-referenced application but that the Office refused to allow claims 31-35 or 37-45.

A Notice of Appeal was filed in the above-referenced application on June 30, 2003.

This Appeal Brief follows the Notice of Appeal. Since this Appeal Brief is being filed by Tuesday, September 2, 2003, it should be deemed to have been filed within two months of the June 30, 2003, mailing date of the Notice of Appeal since August 30, 2003, falls on a Saturday and the following Monday, September 1, 2003, is a federal holiday.

(5) SUMMARY OF THE INVENTION

The above-referenced application teaches a method for forming high-surface area storage capacitor structures. The method includes forming a so-called "storage poly structure" from polysilicon. Fig. 1; page 7, lines 9-11. Following processing to increase the surface area thereof, the storage poly structure will serve as the bottom electrode of the storage capacitor.

The surface area of the storage poly structure is increased by forming a layer of hemispherical-grain (HSG) polysilicon on surface thereof. Fig. 2, page 7, lines 12-24. A mask material is then introduced onto lower elevation portions of the layer of HSG polysilicon, with upper elevation portions thereof remaining exposed. Figs. 3 and 4; page 7, line 25, to page 8,

line 3. Thereafter, the exposed portions of the HSG polysilicon are etched, with the etch continuing on into the underlying storage poly structure. Figs. 8 and 9; page 8, lines 10-23.

The remainder of the storage capacitor may then be fabricated. Fig. 10; page 8, lines 23-26. The remaining HSG polysilicon may remain in place or it may be removed prior to fabricating the remainder of the storage capacitor. *See, e.g.,* page 8, lines 19-23. A dielectric layer may be formed on all of the surfaces of the high surface area storage poly structure. Fig. 10; page 8, lines 23-26. Thereafter, the upper electrode of the storage capacitor may be formed from a suitable conductive material. *Id.*

Various structures are formed at various stages of the process. As one example, an intermediate structure may include a storage poly structure, a confluent layer of HSG polysilicon therover, and a mask material covering lower elevation portions of the HSG polysilicon layer, with upper elevation portions of the HSG polysilicon layer remaining exposed. Fig. 4; page 7, line 26, to page 8, line 2.

Another example of an intermediate structure, which is formed following etching of the HSG polysilicon layer and storage poly, may include the storage poly, recesses formed in the storage poly, and HSG polysilicon on remaining portions of the upper surface of the storage poly. Figs. 8 and 9; page 8, lines 10-23. The remaining portions of the upper surface, and the remaining HSG polysilicon, may impart the storage poly with a contiguous, maze-like, web-like, or honeycomb appearance. Page 5, lines 4-6; Figs. 22-24; page 11, lines 4-25. This example of the intermediate structure may also include mask material over the remaining, lower elevation portions of the HSG polysilicon layer. *See* Fig. 8.

An intermediate structure may also include a dielectric layer over the high surface area storage poly structure. Fig. 10; page 8, lines 23-26. The dielectric layer may line recesses and cover the upper surfaces of the storage poly structure. *Id.* In addition, the dielectric layer may cover the remaining, lower elevation portions of the HSG polysilicon, if they remain in place. Page 8, lines 19-26.

(6) ISSUES

(A) Whether an adequate written description has been provided of the subject matter recited in claims 33, 34, 37-41, 44, and 45, as required by 35 U.S.C. § 112, first paragraph;

(B) Whether claims 31-35 recite subject matter which is novel under 35 U.S.C. § 102(b) over that which is described in U.S. Patent 5,405,799 to Woo et al. (hereinafter "Woo");

(C) Whether claims 35 and 37-45 recite subject matter which is novel under 35 U.S.C. § 102(b) over the subject matter described in U.S. Patent 5,254,503 to Kenney (hereinafter "Kenney"); and

(D) Whether the subject matter to which claim 42 is drawn is novel under 35 U.S.C. § 102(b) over that described in U.S. Patent 5,358,888 to Ahn et al. (hereinafter "Ahn").

(7) GROUPING OF CLAIMS

Claims 31 and 32 are directed to a storage capacitor structure that includes a plurality of contiguous mesas, an element which is not described in any of Woo, Kenney, or Ahn.

Claims 33 and 34 are drawn to a semiconductor capacitor storage poly that includes, among other things, HSG polysilicon on at least some contiguous top surfaces of the storage poly, an additional element which is not described in any of Woo, Kenney, or Ahn. Accordingly, claims 33 and 34 should not be grouped with claims 31 and 32.

Claim 35 recites an intermediate semiconductor capacitor structure which, in addition to elements of claims 31 and 33, includes a mask over an HSG polysilcon layer, another element which is not described in Woo, Kenney, or Ahn or recited in any of claims 31-34. Thus, claim 35 should be grouped separately from each of claims 31-34.

Claims 37-41, 44, and 45 are directed to structures that include a storage poly with HSG polysilicon on upper surfaces thereof, and recesses located laterally between portions of the HSG polysilicon, another element which is not described by Woo, Kenney, or Ahn or recited in any of claims 31-35, 42, or 43. Therefore, claims 37-41, 44, and 45 should be grouped separately from claims 31-35, 42, and 43.

Claim 42 recites a structure which includes a substantially confluent HSG polysilicon layer on a storage poly structure, with elevated portions of the HSG polysilicon layer being exposed through the mask. As this is yet another element which is not described in any of Woo, Kenney, or Ahn, and not described in any of claims 31-35, 37-41, or 43-45, claim 42 should be grouped separately from each of these claims.

Claim 43 is directed to a structure which includes an HSG polysilicon layer on upper surfaces of a storage poly structure and a mask over the HSG polysilicon layer. Recesses in the storage poly structure are exposed through the mask. As this is an element which is not

described in Woo, Kenney, or Ahn and not recited in any of claims 31-35, 37-42, 44, or 45, claim 43 should be grouped separately from each of these claims.

Accordingly, the claims should be grouped as follows:

Group 1 – Claims 31 and 32

Claims 31 and 32 should be grouped together. Claim 31 is the most generic claim of this group. Claim 32 stands and falls with claim 31.

Group 2 – Claims 33 and 34

Claims 33 and 34 should be grouped together. Claim 33 is the most generic claim of this group. Claim 34 stands and falls with claim 33.

Group 3 – Claim 35

Claim 35 should be grouped alone.

Group 4 – Claims 37-41, 44, and 45

Claims 37-41, 44, and 45 should be grouped together. Claim 44 appears to be the most generic claim of this group. Claims 37-41 and 45 stand and fall with claim 44.

Group 5 – Claim 42

Claim 42 should be grouped alone.

Group 6 – Claim 43

Group 43 should be grouped alone.

(8) ARGUMENT

(A) Rejection Under 35 U.S.C. § 112, First Paragraph

Claims 33, 34, 37-41, 44, and 45 stand rejected under the first paragraph of 35 U.S.C. § 112.

(i) Applicable Law

The first paragraph of 35 U.S.C. § 112 provides:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same, and shall set forth the best mode contemplated by the inventor of carrying out his invention.

M.P.E.P. § 2163 provides guidance as to the meaning of the so-called "written description" requirement of 35 U.S.C. § 112, first paragraph:

> An adequate written description of the invention may be shown by any description of sufficient, relevant, identifying characteristics so long as a person skilled in the art would recognize that the inventor has possession of the claimed invention. . .
>
> What is conventional or well known to one of ordinary skill in the art need not be disclosed in detail. . . If a skilled artisan would have understood the inventor to be in possession of the claimed invention at the time of filing, even if every nuance of the claims is not explicitly described in the specification, then the adequate written description requirement is met.

(ii) Analysis

It has been asserted that the specification of the above-referenced application does not provide a written description of leaving remaining portions of an HSG polysilicon layer in place prior to forming a dielectric layer over a high surface area storage poly structure. *See, e.g.,* Advisory Action dated June 26, 2003.

Although the specification does not expressly describe that remaining portions of an HSG polysilicon layer are removed from a storage poly structure prior to the formation of a capacitor dielectric layer thereover, it is respectfully submitted that leaving the HSG polysilicon in place would not be an affirmative act. As such, it is respectfully submitted that one of ordinary skill in the art would readily recognize from the disclosure of the above-referenced application that any remaining portions of the HSG polysilicon layer may remain in place prior to forming a dielectric layer over the exposed surfaces of the storage poly structure.

Moreover, one of ordinary skill in the art would readily understand that it does not matter if any remaining HSG polysilicon remained in place on the storage poly structure, as the HSG polysilicon may have substantially the same electrical conductivity properties as the remaining portions of the underlying polysilicon layer. This is one of the reasons why, following the patterning of the underlying polysilicon layer, the HSG polysilicon does not appear as a separate element. To many of skill in the art, the extra process steps that would be required to remove the HSG polysilicon and clean the structure would be undesirable, as extra process steps increase the likelihood of damage to a device under fabrication and, thus, the probability of device failure.

Further, it has been asserted that since Fig. 10 of the above-referenced application does not depict any remaining HSG polysilicon, the HSG polysilicon must have been removed.

Advisory Action dated June 26, 2003. It is respectfully submitted that Fig. 10 does not depict any remaining HSG polysilicon since leaving the remaining HSG polysilicon in place over the storage poly structure is not a requirement, but rather an option. In any event, such illustration would merely add unnecessary detail to Fig. 10.

Since one of ordinary skill in the art would readily recognize that remaining HSG polysilicon may be either left on or removed from the storage poly structure, it is respectfully submitted that the specification provides an adequate written description of the subject matter recited in claims 33, 34, 37-41, 44, and 45.

Therefore, reversal of the 35 U.S.C. § 112, first paragraph, rejections of claims 33, 34, 37-41, 44, and 45 is respectfully requested.

(B) Rejections Under 35 U.S.C. § 102(b)

Claims 31-35 and 37-45 stand rejected under 35 U.S.C. § 102(b).

(i) Applicable Law

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single reference which qualifies as prior art under 35 U.S.C. § 102. *Verdegaal Brothers v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). The identical invention must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

(ii) References Relied Upon

Woo

Woo describes a structure that, as depicted in FIG. 2 thereof, includes a bottom conductive plate 16, conductive bars 23 thereon, and an upper conductive plate 25 over the bars 23, with the bars 23 electrically connecting the bottom conductive plate 16 and the upper conductive plate 25. At col. 4, lines 9-14, and in FIG. 10, Woo describes and illustrates the bars 23 as comprising a polysilicon layer 18 that "remain[s] as islands of various shapes" which overlie remaining portions of an insulating layer 17, which portions are also referred to in Woo as an insulating layer pattern 19. *See* FIGs. 5 and 6; col. 3, lines 27-38. Thus, the islands of the polysilicon layer 18 of Woo are not connected to one another, or contiguous. Also, the insulating layer 17 of Woo separates the islands of the polysilicon layer 18 from the conductive plate 16 thereof. *See* FIGs. 5 and 6; col. 3, lines 27-38.

Moreover, the polysilicon layer 18 of Woo is not a storage poly—it comprises a mask which is used to form an insulating layer pattern 19. FIG. 6, col. 3, lines 34-38. The insulating layer pattern 19, in turn, is to be subsequently used to define an upper electrode of a capacitor as a layer 20 of conductive material is deposited over and between the insulating layer pattern 19. FIG. 7; col. 3, lines 39-48.

Kenney

Kenney describes storage poly structures and methods for fabricating such structures. In particular, Kenney discloses two methods for forming high surface area storage poly structures, as well as two corresponding intermediate structures.

One intermediate structure of Kenney, shown in FIG. 4 thereof, includes recesses 20 that are formed at areas that are located beneath regions where the high points of surface irregularities 14, such as HSG polysilicon, previously resided. It appears from FIG. 4 that the surface irregularities 14 may have been formed directly on the storage poly structure. FIGs. 1-4 depict the surface irregularities 14 as being spaced apart from one another, not as being contiguous with one another.

Kenney provides for removal of the "mask forming layers" from at least the structure shown in FIG. 4, which "mask forming layers" appear to include both the surface irregularities 14 and the masking layer 16, prior to the formation of a dielectric coating within recesses of the resulting storage poly structure. Col. 4, lines 38-40.

The other intermediate structure, which is depicted in FIG. 5 of Kenney, includes surface irregularities 14, such as HSG polysilicon, which are formed on a layer 12 of silicon dioxide that, in turn, is formed over the storage poly structure. Col. 4, lines 50-55. Thus, the layer of HSG polysilicon shown in FIG. 5 is not in contact with the storage poly structure but, rather, with an intervening layer 12 of silicon dioxide. *Id.* Recesses 21 in the silicon dioxide layer 12 and, thus, in the storage poly structure are formed beneath locations where lower elevation regions of the surface irregularities 14 previously resided. FIG. 5; col. 4, lines 50-55.

Ahn

Ahn teaches a method for manufacturing a capacitor and the structures that result from that method. Among other things, Ahn teaches, at col. 6, lines 31-48, forming HSG polysilicon grains that are "slightly separated from one another, thereby being formed as a group of islands."

(iii) Analysis

Woo

Claims 31-35 stand rejected under 35 U.S.C. § 102(b) for assertedly reciting subject matter which is anticipated by that described in Woo.

Independent claim 31 recites a semiconductor storage capacitor poly that includes downwardly extending recesses and a plurality of contiguous mesas that comprise a plurality of contiguous top surfaces forming a maze-like structure.

The storage electrode 30 shown in FIG. 2 of Woo is an entire storage capacitor, including a lower conductive plate 16, a capacitor dielectric, or insulating pattern 19, that includes bars 23, and an upper conductive plate 20 that includes portions which extend downwardly between bars 23. Thus, it is clear that the polysilicon layer 18 of Woo, which acts merely as a mask for forming insulating pattern 19 from a layer 17 of dielectric material, is not a storage poly. FIGs. 4-7; col. 3, lines 10-48. Therefore, Woo lacks any express or inherent description of a storage poly that includes a plurality of mesas but, rather, describes a mask (formed by polysilicon layer 18) and an insulating layer pattern 19 that include a plurality of islands.

Further, the term "islands" refers to structures which are discrete from one another (Merriam-Webster's Collegiate Dictionary, Tenth Edition, defines "island" as "an isolated group

or area . . ."). The Tenth Edition of Merriam-Webster's Collegiate Dictionary defines "maze" as "a confusing intricate network . . ." As noted at col. 4, lines 12-14 of Woo, the elements of the polysilicon layer 18, and thus the bars 23, are islands. Additionally, FIG. 10 of Woo depicts passageways completely surrounding each of the islands of the polysilicon layer 18, through which portions of the insulating layer 17 are exposed. Accordingly, it is clear from the description of Woo that the islands of the polysilicon layer 18 do not form a confusing intricate network and, thus, are not themselves maze-like. Thus, the islands or bars 23 that are formed (2) from the dielectric layer 17 by using the polysilicon layer 18 as a mask would not be maze-like either.

Further, the term "contiguous" is defined by Merriam-Webster's Collegiate Dictionary, Tenth Edition, as "being in actual contact; touching along a boundary or at a point . . . touching or connected throughout in an unbroken sequence . . ." As used in independent claim 31, it is clear that the mesas themselves must be connected to one another, and that the top surfaces of the mesas must be connected to one another. In contrast, the insulating layer pattern 19 of Woo, which is formed from dielectric layer 17 and has assumed the disconnected island configuration of the overlying mask (polysilicon layer 18), comprises a plurality of disconnected islands or (3) bars 23. While these islands or bars 23 border the material of the upper conductive plate 20, they do not share a border with each other. Moreover, despite the fact that the lower conductive plate 16 serves as a common base or support for the islands or bars of the insulating layer pattern 19, the lower conductive plate 16 does not in any way cause the islands or bars 23 to contact, border, or otherwise become contiguous with one another.

Moreover, as the islands or bars 23 of the insulating layer pattern 19 of Woo are formed prior to deposition of conductive material therearound, the resulting upper conductive plate 20, if it could be properly referred to as a "storage poly," does not include downwardly extending recesses, as recited in independent claim 31.

For these reasons, it is respectfully submitted that Woo does not anticipate each and evey element of independent claim 31 and that, under 35 U.S.C. § 102(b), independent claim 31 recites subject matter which is allowable over that described in Woo.

Claim 32 is allowable, among other reasons, as depending from claim 31, which is allowable.

Independent claim 33 also recites a semiconductor capacitor storage poly. The capacitor storage poly of independent claim 33 includes downwardly extending recesses, a plurality of contiguous webs that comprise contiguous top surfaces, and HSG polysilicon on at least some of the contiguous top surfaces.

Again, the polysilicon layer 18 of Woo is not a storage poly—it is a mask which is used to form an insulating layer pattern 19 that is to be subsequently used to define a storage poly (conductive layer 20).

Furthermore, Woo includes no express or inherent description of a storage poly structure that includes downwardly extending recesses. Rather, the conductive layer 20 if Woo, which is the only feature described therein that could be reasonably referred to as a "storage poly," is formed over the islands or bars 23 of an insulating layer pattern 19 have already been formed. Thus, the structures that are described in Woo could not include any recesses that extend

downwardly into the conductive layer 20 but, rather, recesses that extend upwardly into the conductive layer 20 and that are instantaneously filled with the islands or bars 23.

Moreover, Woo lacks any express or inherent description of a capacitor storage poly that includes a plurality of contiguous webs that comprise a plurality of contiguous top surfaces. Instead of contiguous webs, the description of Woo is limited to a polysilicon layer 18 which includes "*islands* of various shapes." Col. 4, lines 12-14 (emphasis supplied). When the underlying dielectric layer 17 is patterned to form an insulating layer pattern 19, the islands or bars 23 of the insulating layer pattern 19 assume the shapes of the islands of the mask (*i.e.*, the polysilicon layer 18). As the term "islands" refers to structures which are discrete from one another, and since Woo does not describe that the islands of polysilicon layer 18 may be connected to or share a border with one another, it is clear that none of the islands of polysilicon layer 18, the islands or bars 23 of the insulating layer pattern layer 19, or their top surfaces is contiguous with any other island or bar.

Accordingly, it is respectfully submitted that Woo does not anticipate each and every element of independent claim 33. It is, therefore, submitted that, under 35 U.S.C. § 102(b), independent claim 33 recites subject matter which is allowable over that described in Woo.

Claim 34 is allowable, among other reasons, as depending from claim 33, which is allowable.

Independent claim 35 recites an intermediate semiconductor capacitor structure that includes a storage poly structure, a contiguous HSG polysilicon layer on and in contact with the

storage poly structure, and a mask over the HSG polysilicon layer. Recesses in the storage poly structure are exposed through the contiguous HSG polysilicon layer and the mask.

As Woo describes that the islands of the polysilicon layer 18 depicted in FIG. 10 are located over remaining portions of a second insulating layer 17, or an insulating layer pattern 19, they cannot be on and in contact with a storage poly structure, as recited in independent claim 35.

Furthermore, Woo neither expressly nor inherently describes a storage poly structure with downwardly extending recesses. Again, the description of Woo is limited to an insulating layer pattern 19 with downwardly extending recesses, which recesses are to be subsequently filled with portions of a conductive layer 20, which would comprise the storage poly structure.

In addition, Woo does not expressly or inherently describe an HSG polysilicon layer that is on and in contact with a storage poly structure. Rather, the description of Woo is limited to a polysilicon layer 18 that overlies and contacts an insulating layer 17 that is on a bottom conductive plate 16. *See* FIGs. 4 and 5; col. 3, lines 10-33.

Further, as explained above, the islands of the polysilicon layer 18, which are, by definition, separate, cannot be contiguous with one another. Nor could the islands or bars 23 of the insulating layer pattern 19, which is formed by use of the polysilicon layer 18 as a mask and assumes the shape of the polysilicon layer 18, share a border or otherwise be contiguous with one another. The mere fact that a lower conductive plate 16 serves as a base or a support for the islands or bars 23 in no way causes the islands or bars 23 to share borders or otherwise become contiguous with one another.

Therefore, it is respectfully submitted that Woo does not anticipate each and every element of independent claim 35 and that, under 35 U.S.C. § 102(b), independent claim 35 is allowable over Woo.

Kenney

Claims 35 and 37-45 stand rejected under 35 U.S.C. § 102(b) for reciting subject matter which is purportedly anticipated by that described in Kenney.

Independent claim 35 recites an intermediate semiconductor capacitor structure that includes a storage poly structure, a contiguous HSG polysilicon layer on and in contact with the storage poly structure, and a mask over the HSG polysilicon layer. Recesses in the storage poly structure are exposed through the contiguous HSG polysilicon layer and the mask.

Kenney neither expressly nor inherently describes that either the structure shown in FIG. 4 thereof or the structure shown in FIG. 5 thereof includes a contiguous layer of HSG polysilicon. Further, FIGs. 1-4 depict the surface irregularities 14, which may comprise HSG polysilicon, as being spaced apart from one another, not as being contiguous with one another. More specifically, as shown in FIG. 4, the HSG polysilicon 14 (FIG. 1) that remains on the silicon dioxide masking layer 12 are laterally spaced apart from one another and, thus, do not share borders with each other. While the underlying substrate 10 serves as a base or support for the separated portions of the masking layer 12 and the HSG polysilicon 14, it does not cause separate islands of the remaining HSG polysilicon 14 to share borders with one another. It is, therefore, abundantly clear that the remaining portions of HSG polysilicon 14 that are shown in FIG. 4 are not contiguous with one another.

The structure shown in FIG. 5 of Kenney does not include a contiguous layer of HSG polyslicon on and in contact with a storage poly structure *and* a mask over the HSG polysilicon layer. More specifically, Kenney lacks any express or inherent description that the structure shown in FIG. 5 thereof ever requires or includes a mask. Moreover, Kenney lacks any express or inherent description that the structure shown in FIG. 5 includes a contiguous layer of HSG polysilicon. Instead, if HSG polysilicon were used, lower-elevation regions thereof would have been removed to form recesses, with only the spaced-apart (*i.e.,* not contiguous), upper regions of the HSG polysilicon remaining. Further, the layer of HSG polysilicon shown in FIG. 5 is not in contact with the storage poly structure but, rather, with an intervening layer 12 of silicon dioxide. Col. 4, lines 50-55.

For these reasons, it is respectfully submitted that Kenney does not expressly or inherently describe an embodiment which anticipates each and every element of independent claim 35. Thus, under 35 U.S.C. § 102(b), the subject matter to which independent claim 35 is drawn is allowable over the subject matter described in Kenney.

Independent claim 37 recites an intermediate semiconductor memory cell structure that includes a storage poly structure, a plurality of contiguous low elevation regions of an HSG polysilicon layer on and in contact with the storage poly structure, recesses formed in the storage poly structure laterally between the low elevation regions, and dielectric material at least lining the recesses.

In FIGs. 1-4 of Kenney, the low-elevation regions of the surface irregularities 14, which may or may not comprise HSG polysilicon, are shown as being spaced apart from one another,

not as being contiguous with each other. *See, e.g.,* FIGs. 1-4, which depict the masking layer 12 as being exposed between adjacent grains of the HSG polysilicon 14. As Kenney lacks any express or inherent description of a structure that includes a plurality of contiguous low elevation regions of an HSG polysilicon layer, it is respectfully submitted that Kenney does not anticipate each and every element of independent claim 37.

Therefore, it is respectfully submitted that, under 35 U.S.C. § 102(b), independent claim 37 is drawn to subject matter which is allowable over that described in Kenney.

Independent claim 38 recites a semiconductor memory cell structure that includes "regions of hemispherical-grain polysilicon on at least portions of an upper surface of said storage poly structure . . . and a dielectric layer substantially coating an upper surface of said storage poly structure and substantially lining each of said plurality of recesses".

Kenney does not include any express or inherent description of a semiconductor memory cell structure that includes HSG polysilicon on the top surfaces of a storage poly structure, the recesses of which are substantially coated with a dielectric layer. To the contrary, at col. 4, lines 38-40, Kenney provides for removal of the "mask forming layers" from at least the structure shown in FIG. 4, which "mask forming layers" appear to include both the surface irregularities 14 and the masking layer 16, prior to the formation of a dielectric coating within recesses of the resulting storage poly structure.

With respect to the description that accompanies FIG. 5 of Kenney, it is clear that if HSG polysilicon were used to form the surface irregularities 14, that the HSG polysilicon would not be located on a storage poly structure (*e.g.,* substrate 10) but, rather, on a layer 12 of silicon dioxide

that, in turn, has been placed on the storage poly structure (*e.g.*, substrate 10). Col. 4, lines 50-55.

For these reasons, it is respectfully submitted that Kenney does not anticipate each and every element of independent claim 38 and, thus, that, under 35 U.S.C. § 102(b), independent claim 38 is allowable over Kenney.

Claims 39-41 are each allowable, among other reasons, as depending from claim 38, which is allowable.

Independent claim 42 recites an intermediate semiconductor capacitor structure that includes a storage poly structure, a substantially confluent HSG polysilicon layer on the storage poly structure, and a mask positioned over the HSG polysilicon layer. Elevated portions of the HSG polysilicon layer are exposed through the mask.

Kenney lacks any express or inherent description of an intermediate structure that includes a substantially confluent layer of HSG polysilicon. In particular, Kenney illustrates that the surface irregularities 14 are isolated from one another, meaning that they are not substantially confluent (*i.e.*, flow or come together; *see* Merriam-Webster's Collegiate Dictionary, Tenth Edition). Kenney also lacks any express or inherent description that both the surface irregularities 14 and the underlying region 12 may both be formed from HSG polysilicon, which is the only other way that Kenney could include a substantially confluent HSG polysilicon layer, as required by independent claim 42.

Further, the mere fact that a substrate 10, which clearly does not comprise HSG polysilicon (*see* col. 3, line 68, to col. 4, line 17; col. 4, lines 45-47 and 50-55) that underlies the HSG polysilicon of Kenney is confluent does not make the HSG polysilicon itself confluent.

For these reasons, it is respectfully submitted that Kenney does not anticipate each and every element of independent claim 42. Accordingly, it is respectfully submitted that, under 35 U.S.C. § 102(b), independent claim 42 is drawn to subject matter which is allowable over the subject matter described in Kenney.

Independent claim 43 also recites an intermediate semiconductor capacitor structure. The intermediate semiconductor capacitor structure of independent claim 43 includes a storage poly structure with recesses therein, remaining portions of an HSG polysilicon layer substantially overlying upper portions of the storage poly structure, and a mask positioned over the HSG polysilicon layer. The mask is located laterally between the recesses in the storage poly structure, with the recesses being exposed therethrough, and is substantially spaced apart from the storage poly structure by way of the remaining portions of HSG polysilicon layer.

Kenney neither expressly nor inherently describes an intermediate semiconductor capacitor structure that includes portions of an HSG polysilicon layer that substantially overlie upper portions the storage poly structure or that the mask thereof is substantially spaced apart from storage poly structure by way of the remaining portions of the HSG polysilicon layer described therein. Instead, FIGs. 2-4 of Kenney show a mask 16 and an underlying silicon dioxide masking layer 12 which are located directly over a substrate 10, not separated therefrom by way of HSG polysilicon.

Therefore, it is respectfully submitted that Kenney does not anticipate each and every element of independent claim 43 and, thus, that, under 35 U.S.C. § 102(b), independent claim 43 is allowable over Kenney.

Independent claim 44 recites an intermediate semiconductor capacitor structure that includes a storage poly structure with recesses therein, an HSG polysilicon layer on at least portions of the storage poly structure, and dielectric material lining at least the recesses.

Again, Kenney lacks any express or inherent description of an intermediate semiconductor capacitor structure which includes both dielectric material lining the recesses that are formed in a storage poly structure and HSG polysilicon on portions of the storage poly structure.

Therefore, under 35 U.S.C. § 102(b), independent claim 44 is allowable over Kenney.

Independent claim 45 is directed to an intermediate semiconductor memory cell structure that includes a storage poly with recesses therein, low elevation regions of an HSG polysilicon layer substantially covering an upper surface of the storage poly structure, and dielectric material at least lining the recesses.

Kenney neither expressly nor inherently describes an intermediate semiconductor capacitor structure which includes both dielectric material lining the recesses that are formed in a storage poly structure and HSG polysilicon that substantially covers an upper surface of the storage poly structure.

Accordingly, under 35 U.S.C. § 102(b), independent claim 45 is allowable over Kenney.

Ahn

Claim 42 stands rejected under 35 U.S.C. § 102(b) for reciting subject matter which is been asserted to be anticipated by Ahn.

Independent claim 42 recites an intermediate semiconductor capacitor structure that includes a storage poly structure, a substantially confluent HSG polysilicon layer on the storage poly structure, and a mask positioned over the HSG polysilicon layer. Elevated portions of the HSG polysilicon layer are exposed through the mask.

Again, "confluent" means "flowing or coming together" (Merriam-Webster's Collegiate Dictionary, Tenth Edition). Ahn teaches that the HSG polysilicon layer thereof includes islands that are separated, or isolated, from one another. This is apparent from FIGs. 7, 18, and 23 of Ahn, which depict HSG polysilicon layers 80 through which an underlying layer 50 is partially exposed. *See also,* col. 6, lines 44-48. Therefore, Ahn does not expressly or inherently describe a structure which includes a substantially confluent HSG polysilicon layer; *i.e.,* that the grains thereof flow or come together.

Accordingly, it is respectfully submitted that, under 35 U.S.C. § 102(b), independent claim 42 is allowable over Ahn.

For the foregoing reasons, it is respectfully requested that the 35 U.S.C. § 102(b) rejections of claims 31-35 and 37-45 be reversed.

(9) APPENDIX

A copy of claims 31-35 and 37-45 as last amended is appended hereto as the "Appendix."

(10) CONCLUSION

It is respectfully submitted that:

(A) The specification of the above-referenced application provides an adequate written description for the subject matter recited in claims 33, 34, 37-41, 44, and 45, as required by 35 U.S.C. § 112, first paragraph;

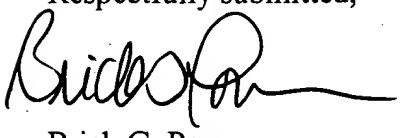
(B) Claims 31-35 recite subject matter which is novel under 35 U.S.C. § 102(b) over that which is described in Woo;

(C) Claims 35 and 37-45 recite subject matter which is novel under 35 U.S.C. § 102(b) over the subject matter described in Kenney; and

(D) The subject matter to which claim 42 is drawn is novel under 35 U.S.C. § 102(b) over that described in Ahn.

Accordingly, the reversal of the claim rejections and the allowance of claims 31-35 and 37-45 are respectfully solicited.

Respectfully submitted,



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APPENDIX

31. A semiconductor capacitor storage poly, comprising:

downwardly extending recesses; and

a plurality of contiguous mesas comprising a plurality of contiguous top surfaces forming a maze-like structure.

32. The storage poly of claim 31, wherein said mesas extend in the X, Y and Z coordinates.

33. A semiconductor capacitor storage poly, comprising:

downwardly extending recesses;

a plurality of contiguous webs comprising a plurality of contiguous top surfaces forming a maze-like structure; and

hemispherical-grain polysilicon on at least some of said plurality of contiguous top surfaces.

34. The storage poly of claim 33, wherein said webs extend in the X, Y and Z coordinates.

35. An intermediate semiconductor capacitor structure, comprising:

a storage poly structure comprising a plurality of contiguous mesas with recesses therebetween;

a contiguous hemispherical-grain polysilicon layer on said storage poly structure and in contact therewith; and

a mask over said hemispherical-grain polysilicon layer, said recesses being exposed through said contiguous hemispherical-grain polysilicon layer and said mask.

37. An intermediate semiconductor memory cell structure, comprising:

a storage poly structure;

a plurality of contiguous low elevation regions of a hemispherical-grain polysilicon layer on said storage poly structure;

recesses formed in said storage poly structure and located laterally between said plurality of contiguous low elevation regions of said hemispherical-grain polysilicon layer; and

dielectric material at least lining the recesses.

38. A semiconductor memory cell structure, comprising:

a storage poly structure;

regions of hemispherical-grain polysilicon on at least portions of an upper surface of said storage poly structure;

a plurality of recesses extending into said storage poly structure, at least some recesses of said plurality of recesses being located laterally between said regions of hemispherical-grain polysilicon; and

and a dielectric layer substantially coating an upper surface of said storage poly structure and substantially lining each of said plurality of recesses.

39. The semiconductor memory cell structure of claim 38, further comprising a cell poly structure over said dielectric layer.

40. The semiconductor memory cell structure of claim 38, wherein said storage poly structure comprises a web-like structure comprising a plurality of contiguous top surfaces.

41. The semiconductor memory cell structure of claim 38, wherein at least some of said plurality of recesses extend into said storage poly structure.

42. An intermediate semiconductor capacitor structure, comprising:

a storage poly structure;

a substantially confluent hemispherical-grain polysilicon layer on said storage poly structure; and

a mask positioned over said substantially confluent hemispherical-grain polysilicon layer, elevated portions of said hemispherical-grain polysilicon layer being exposed through said mask.

43. An intermediate semiconductor capacitor structure, comprising:

a storage poly structure including recesses therein;

remaining portions of a hemispherical-grain polysilicon layer substantially overlying upper portions of said storage poly structure; and

a mask positioned over said hemispherical-grain polysilicon layer, laterally between said recesses, and substantially spaced apart from said storage poly structure by said remaining portions of said hemispherical-grain polysilicon layer, said recesses in said storage poly structure being exposed through said mask.

44. An intermediate semiconductor capacitor structure, comprising:

a storage poly structure with recesses therein;

a hemispherical-grain polysilicon layer on at least portions of the storage poly structure; and